MCDP6000

USB Type-C DP Alt-Mode Switching Retimer

Data Brief

KDB-MCDP6000-101

Rev. 1.0.1
Features

- Integrated USB Type-C DisplayPort alternate mode lane switch to support
  - Flip-ability of USB Type-C
  - Simultaneous USB3.1 Enhanced SuperSpeed (ESS) and 2 lane DP1.3
  - 4/2/1-Lane DP1.3 (RBR/HBR/HBR2/HBR3)

- Power Supply Voltages
  - 1.8 V for I/O, 1.2 V for core or 1.8V single
  - 3.3 V for Direct Connect Interface (DCI) output

- USB3.1 Appendix.E Compliant Retimer
  - 5 Gbps and 10 Gbps support
  - Link training participation
  - Spread-spectrum clocking as per USB 3.1 standard
  - LFPS polling and processing
  - LFPS Based PWM support
  - Pass-Through / Local loopback
  - Loopback BERT for USB 3.1 SS
  - Lane polarity inversion
  - BLR (Bit-Level Retimer) for SS mode
    - Low latency data path
    - Link layer snooping
      - 8b/10b coding
      - De-scrambler
      - Link power management support
  - SRIS (Separate Reference clock Independent SSC) for SSP mode
    - 128b/132b coding
    - Scrambler / De-scrambler
    - Link power management support
    - SKP OS handling / Elastic buffer for USB for clock offset compensation
    - DC balance tracking / control
    - PTM / LDM handling
    - Error correction
  - Transmitter Emphasis
    - 3-tap FIR TXEQ for SSP
    - 2-tap TXEQ for SS
  - Adaptive Receiver Equalization
    - 4-tap DFE + CTLE for SSP
    - CTLE for SS
  - Support of custom PHY configuration

- DP1.4 Compliant Repeater
  - Data rate 1.62 Gbps / 2.7 Gbps / 5.4 Gbps / 8.1 Gbps
  - LT-tunable repeater
  - Transparent mode / Non-transparent mode support
  - AUX_CH transaction snooping
  - DP1.4 Compliant Retimer DPCD registers
  - 8b/10b coding
  - Pattern generator and Error Checker
  - Down-spreading of link clock
  - Error detection
  - Adjustable TXEQ during the link training through AUX_CH
  - Adaptive equalizer with CTLE and DFE
    - 4-tap DFE + CTLE for HBR3
    - CTLE for HBR2 / HBR / RBR
  - Support of custom PHY configuration

- I2C slave to configure the integrated lane mapping and operation mode
  - Support up to 4 unique I2C device ID

- Configuration pins for the integrated lane switch and operation mode
  - Can be optionally enabled by I2C

- DCI interface support

- Low Power Operation (Dual-Supply)
  - 570 mW in USB3.1 SSP + Two lanes of DisplayPort HBR3 operation with 1.2 V and 1.8 V power supply
  - 850 uW in standby mode (T.B.D.)

- ESD Specification
  - HS Signals : 1 KV HBM
  - Low-Speed Signals : 2 KV HBM

- Package
  - 46 Ex-VQFN (6.5 mm x 4.5 mm)
Applications

- Desktop PC / Notebook / Tablet / Smartphone motherboard enabling USB Type-C DP alternate mode

Figure 1. MCDP6000 System Block Diagram
1. Description

The MCDP6000 is a low power USB3.1 and DisplayPort1.3 repeater device with an integrated USB Type-C switch targeted for desktop / mobile PC motherboard-down application.

The USB3.1 retimer supports both SuperSpeed (SS) bit rate (5Gbps), and SuperSpeedPlus (SSP) data rate (10Gbps). The USB3.1 retimer includes the link layer function and LTSSM and RTSSM to participate in the link training. The MCDP6000 supports SS mode with BLR (Bit-Level Retimer) and SSP mode with SRIS (Separate Reference clock Independent SSC). The MCDP6000 supports link power management with Ux entry and exits in both SS and SSP modes. In addition, the MCDP6000 supports the link state and link quality maintenance, compensates the clock offset between the downstream port and the upstream port, detects errors, and corrects single symbol error in framing order sets, single bit block header error, and single or double-bit SKP symbol error in SSP mode. It also supports spread spectrum clocking (SSC) to minimize EMI and the low frequency periodic signaling (LFPS). The transmitter employs 3-tap FIR-based transmitter equalizer for SSP operation and fixed transmitter equalizer ranging from 3 dB to 4 dB for SS operation. The receiver employs an adaptive Continuous Time Linear Equalizer (CTLE) and a 4-tap Decision Feedback Equalizer (DFE). Both the transmitter equalizer and the receiver equalizer are configurable through the I2C register while proper settings to comply with USB 3.1 standard are provided in default.

The DP1.4 repeater supports 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps data rates. The following use cases are supported.

### Table 1. DP1.4 Repeater Mode

<table>
<thead>
<tr>
<th>Tunability</th>
<th>Mode</th>
<th>AUX_CH Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT tunable PHY Repeater</td>
<td>Non-transparent mode</td>
<td>Sample, Manipulate, and Forward to snoop or respond</td>
</tr>
<tr>
<td></td>
<td>Transparent mode</td>
<td>Sample and Forward to snoop</td>
</tr>
<tr>
<td>Snooping PHY Repeater</td>
<td>Transparent mode with the transmitter adjustment according to a request from sink side</td>
<td>Snooping</td>
</tr>
</tbody>
</table>

The DP1.4 repeater implements AUX_CH snooping function of DPCD addresses defined in the standard as well as the LT-tunable PHY Repeater DPCD registers. The DP1.4 repeater can support up to 0.5% downspread link rate. The transmitter employs TXEQ, which adjust its pre-emphasis level according to either the AUX_CH transaction during the link training or the I2C interface. The receiver employs a fully adaptive Continuous Time Linear Equalizer (CTLE) and 4-tap Decision Feedback Equalizer (DFE).
The parameter sets to support the amplitude level and the pre-emphasis level defined in DP 1.4 standard are provided in default while these parameter sets are configurable to support customization.

The MCDP6000 operating mode can be configured through the I2C interface in default. It can be optionally configured through the 3 configuration pins by enabling this feature through I2C. These interfaces can be controlled from an external Power Delivery (PD) controller or microcontroller to set the plug orientation and the pin mapping of the USB Type-C DP Alt-mode. The MCDP6000 can operate at one of three power supply options: three supplies: 3.3 V, 1.8 V, and 1.2 V; two supplies: 3.3 V and 1.8 V, 1.8V and 1.2V or one supply: 1.8 V.

The power consumption with the three supply voltages is:

1. 570 mW with an active 4 lane retimer (USB3.1 SSP TX/RX and DP 2 lanes HBR2)
2. 850 uW in stand-by state

The MCDP6000 is offered in a 46-pin, 6.5 mm x 4.5 mm Ex-VQFN package.

2. Application Overview

The target application of MCDP6000 is the Desktop PC / Notebook / Tablet / Smartphone motherboard enabling USB Type-C DP alternate mode.

The MCDP6000 resides next to the DisplayPort source (CPU/GPU) device, the USB 3.1 host or dual-role device, and the Power Delivery (PD) controller on a same PCB with copper tracks connecting directly to these devices. High speed serial interface tracks are typical microstrip lines with controlled impedance of 100 ohm. The MCDP6000 communicates with these devices through either I2C interface, 3 configuration pins or AUX_CH. In default, the operating mode and the plug orientation are controlled by the PD controller or the Embedded Controller (EC) through the I2C. When the DisplayPort link is discovered by the PD controller, the link training is initiated by the DP source through the AUX_CH.

Figure 2. MCDP6000 Motherboard-Down Use Case
Figure 3. MCDP6000 System Block Diagram (AUX_CH Sniffing Topology)

Motherboard

CPU

3.3V 1.8V 1.2V

DCI

USB SSRX
USB SSTX
DP ML0
DP ML1
DP ML2
DP ML3
AUX_CH
HPO

MCDP6000

V18 V12

USB SSRX
USB SSTX
DP ML0
DP ML1
DP ML2
DP ML3
AUX_CH (Sniffing)

GND XTAL IDC Config

PD controller

Power Management Unit

VBUS To MB

XTAL

On/off switch

3.3V

1.8V

1.2V

Figure 4. MCDP6000 System Block Diagram (AUX_CH typical topology)

Motherboard

CPU

3.3V 1.8V 1.2V

DCI

USB SSRX
USB SSTX
DP ML0
DP ML1
DP ML2
DP ML3
AUX_CH
HPO

MCDP6000

V18 V12

USB SSRX
USB SSTX
DP ML0
DP ML1
DP ML2
DP ML3
AUX_CH

GND XTAL IDC Config

PD controller

Power Management Unit

VBUS To MB

XTAL

On/off switch

3.3V

1.8V

1.2V
3. Ordering Information

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<th>Part Number</th>
<th>Description</th>
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<tr>
<td>MCDP6000B0E</td>
<td>Engineering sample. (QFN)</td>
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<td>All updates to address Appendix.E update will be implemented.</td>
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<tr>
<td>MCDP6000B0C</td>
<td>Commercial Sample of B0 version (QFN)</td>
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<tr>
<td>MCDP6000B0</td>
<td>Production version (QFN)</td>
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4. Revision history

Table 2. Document revision history

<table>
<thead>
<tr>
<th>Revision</th>
<th>Revision Date</th>
<th>Summary of Change</th>
<th>Section/Page Changed</th>
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<tr>
<td>1.0.0</td>
<td>April 27th, 2017</td>
<td>• Initial Release</td>
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</tr>
<tr>
<td>1.0.1</td>
<td>May 15th, 2017</td>
<td>• Remove information not related to MCDP6000</td>
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